2007 Microprocessor Forum

The New Era of Scaling for Energy Efficient Processors

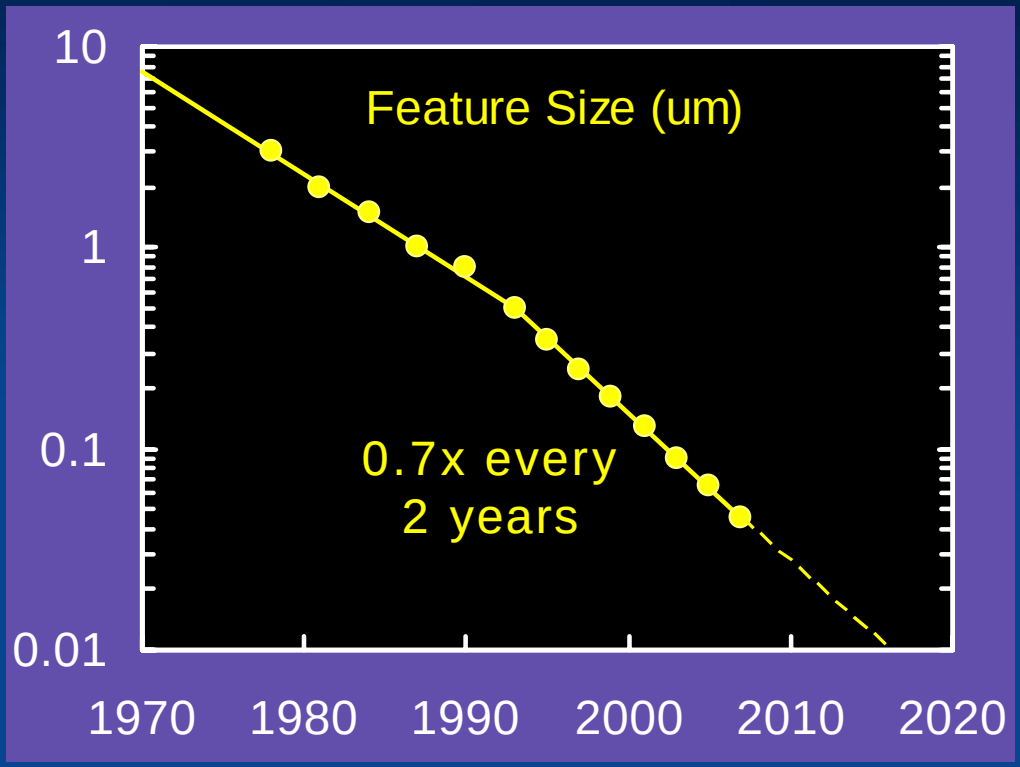
Mark Bohr

Intel Senior Fellow

Logic Technology Development

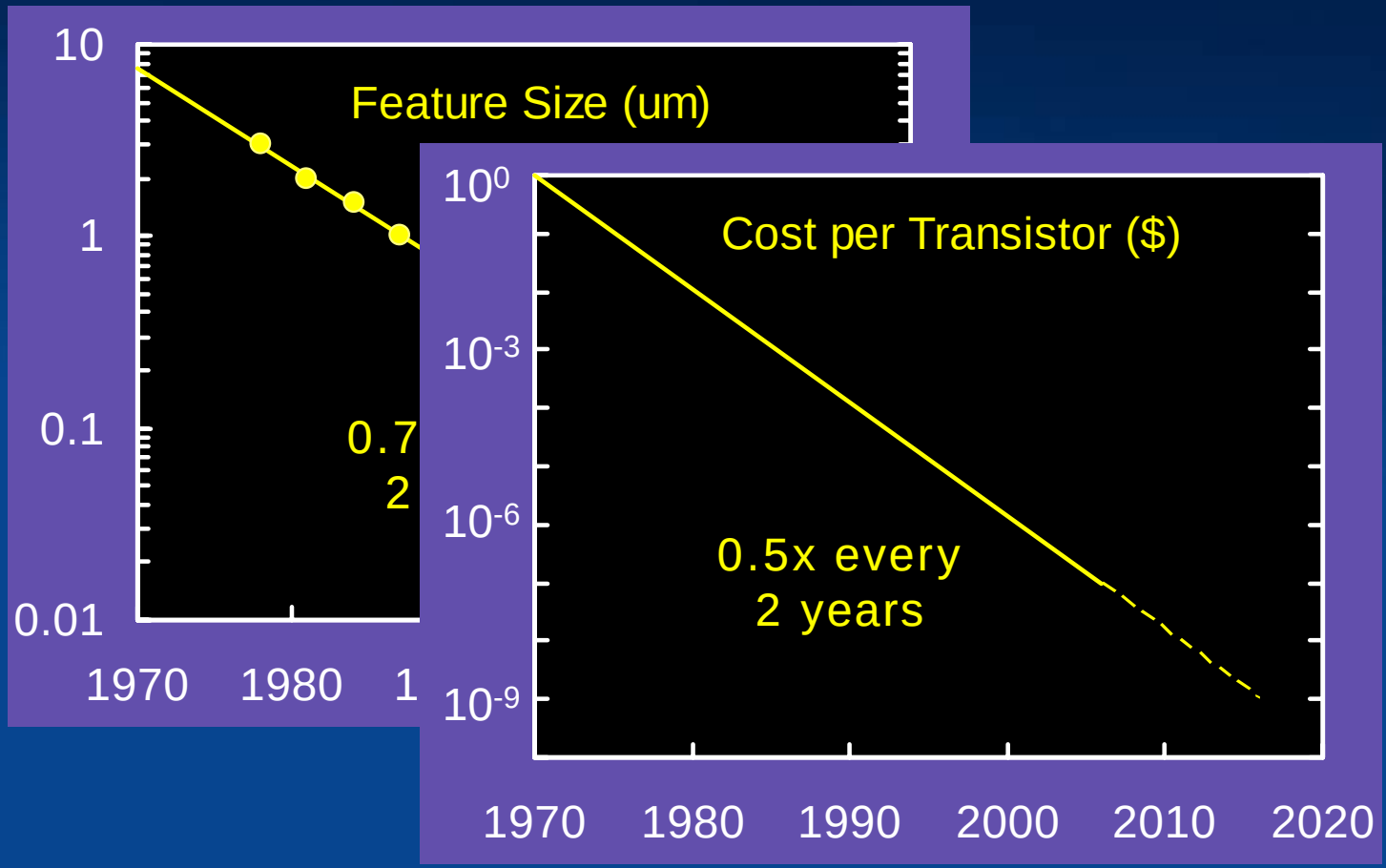
May 22, 2007

Delivering Moore's Law



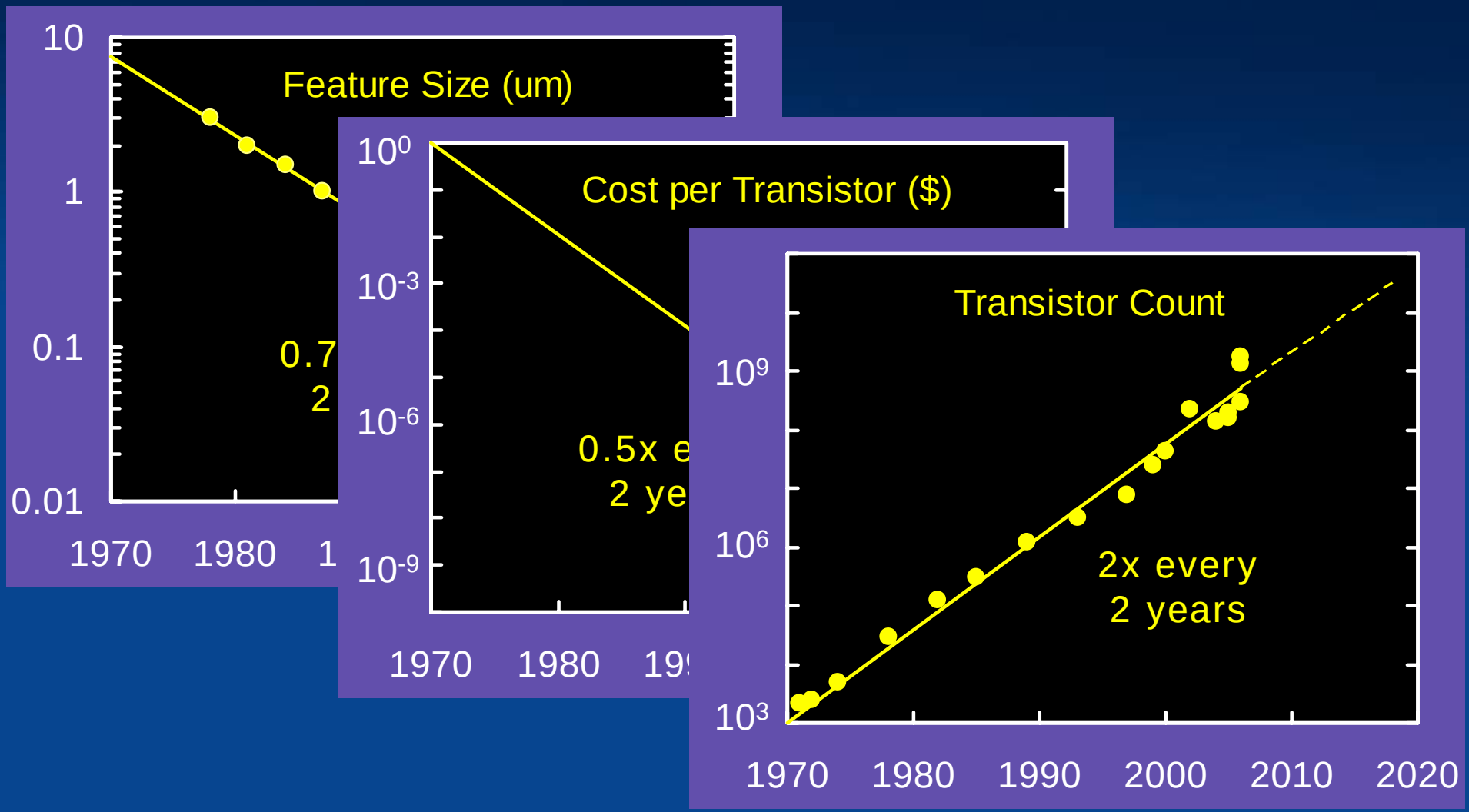
Smaller dimensions

Delivering Moore's Law



Provide lower cost per transistor

Delivering Moore's Law



Enables more transistors and increased performance

Intel's Silicon R&D Pipeline

Identify Ideas/Options

Components Research
- Oregon
- California
- Arizona

External
- Consortia
- Universities

Select Features Make it Work

Logic Technology Development
- Oregon

High Volume Manufacturing

- United States
- Ireland
- Israel
- China (2010)

3 phases of R&D Pipeline

Intel's Silicon R&D Pipeline

Identify Ideas/Options

Components Research

Oregon
California
Arizona

External

Consortia
Universities

Select Features Make it Work

Logic Technology Development

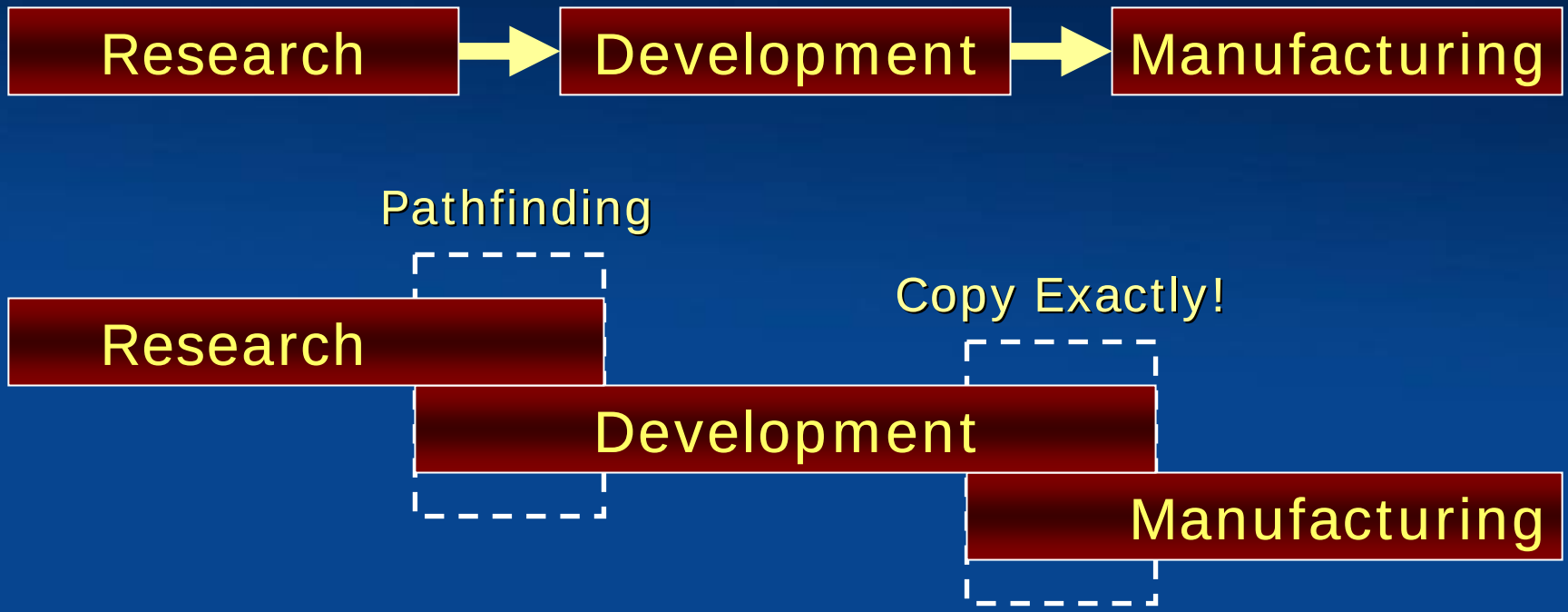
Product Design

High Volume Manufacturing

United States
Ireland
Israel
China (2010)

Close collaboration with product design groups during development

Intel's Silicon R&D Pipeline



Organizational overlap is a critical component of R&D Pipeline

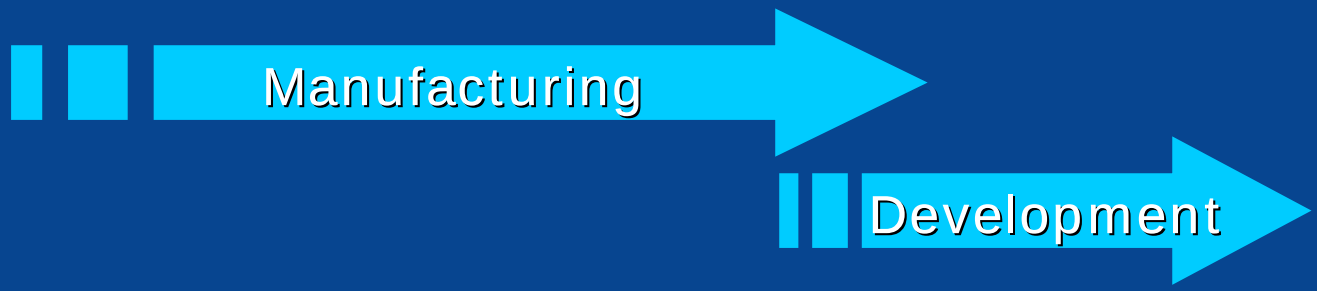
Intel's Silicon R&D Pipeline

Research Development Manufacturing

Continuous flow of new technologies from research to development to manufacturing

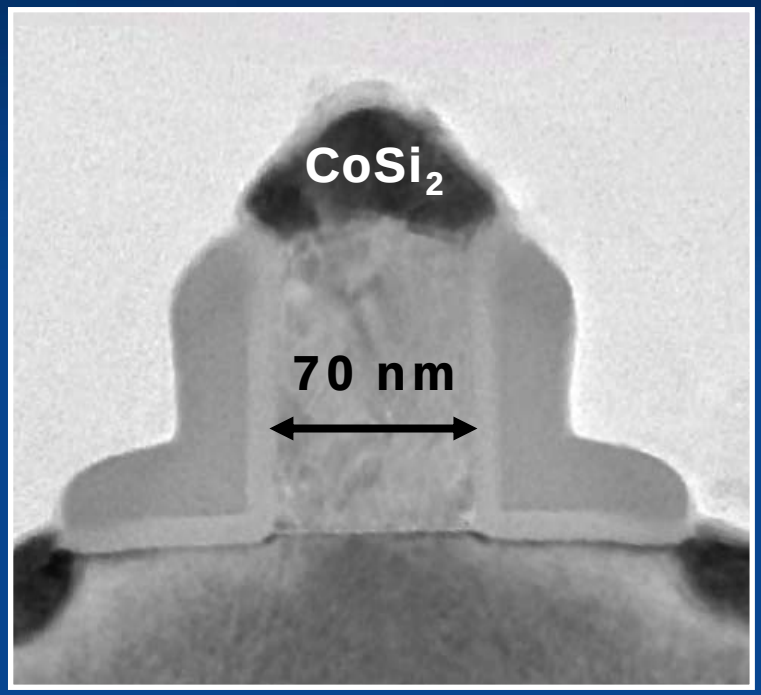
Logic Technology Evolution

Process Name	P860	P1262	P1264	P1266	P1268
Lithography	130nm	90nm	65nm	45nm	32nm
1st Production	2001	2003	2005	2007	2009
Wafer (mm)	200/300	300	300	300	300



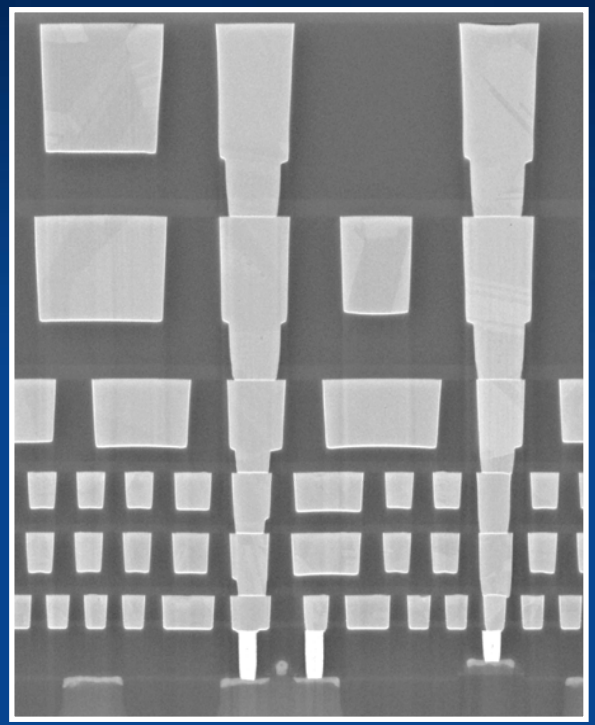
130 nm Technology - 2001

Transistors



1.5 nm gate oxide

Interconnects

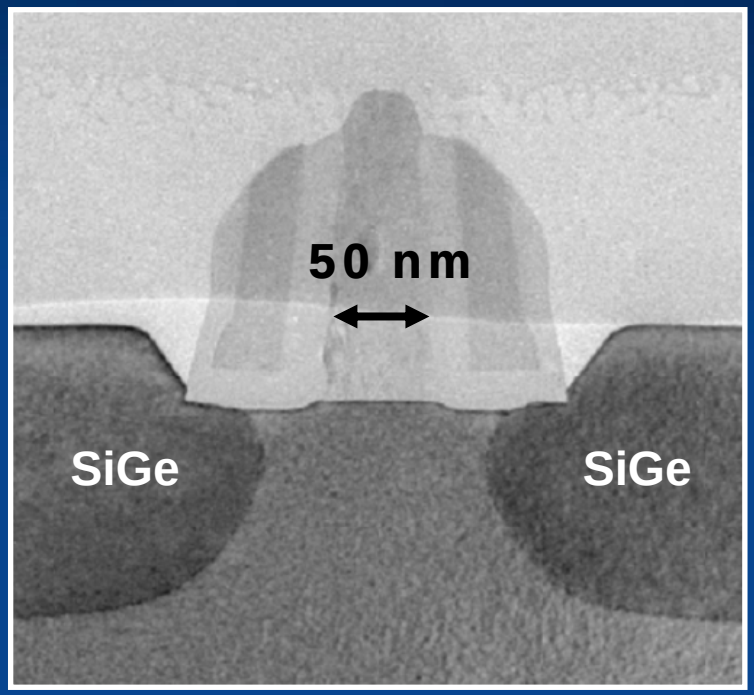


6 copper layers

SiOF dielectric

90 nm Technology - 2003

Transistors

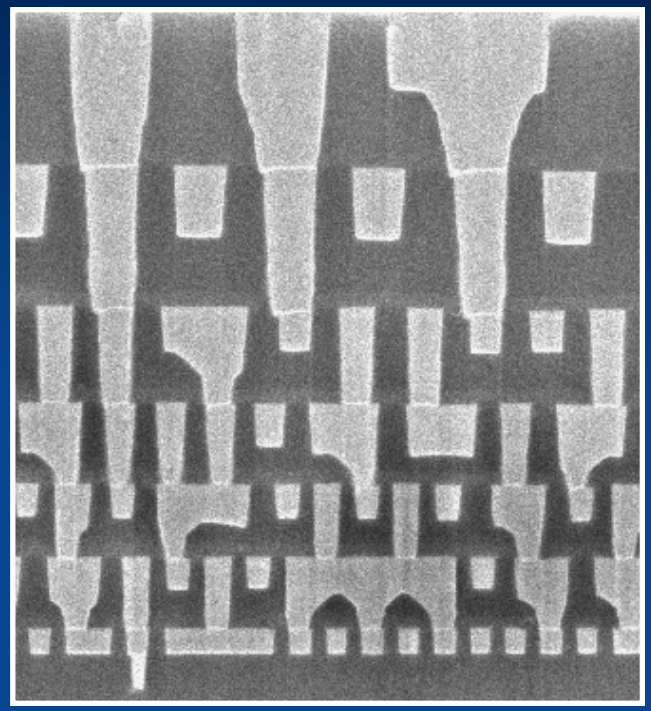


1.2 nm gate oxide

NiSi for low resistance

SiGe strained silicon technology

Interconnects

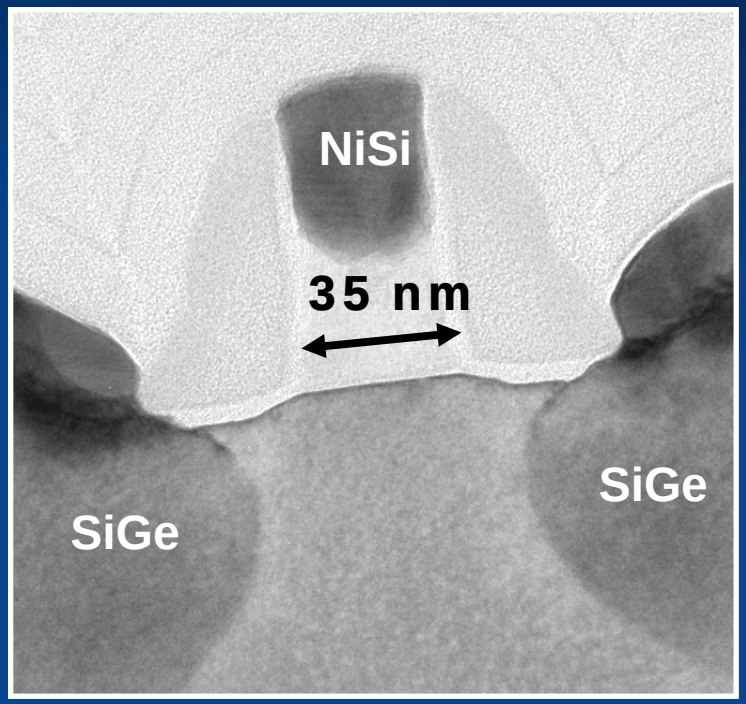


7 copper layers

Low-k carbon-doped oxide

65 nm Technology - 2005

Transistors

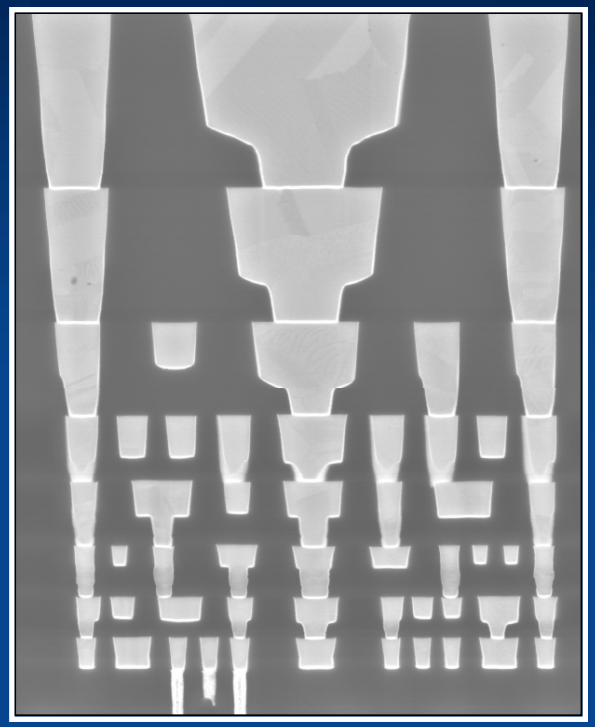


1.2 nm gate oxide

2ND gen. SiGe strained silicon

Industry-leading performance

Interconnects

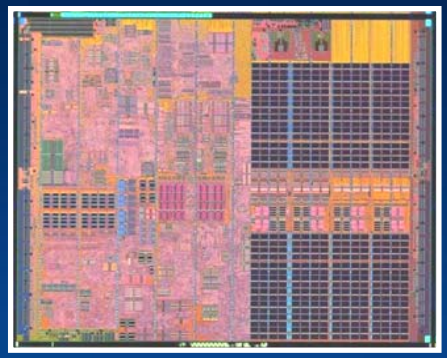


8 copper layers

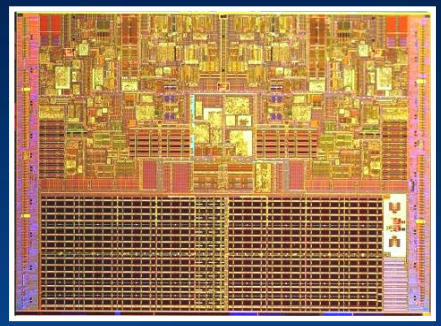
Low-k carbon-doped oxide

SiCN etch-stop layer

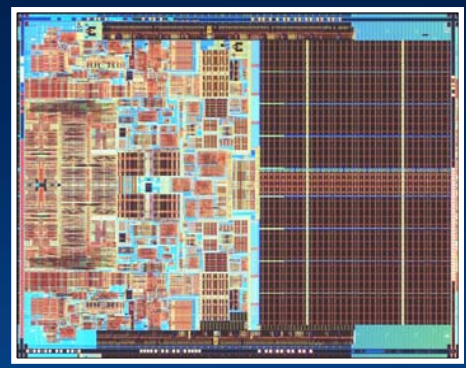
65 nm Microprocessors



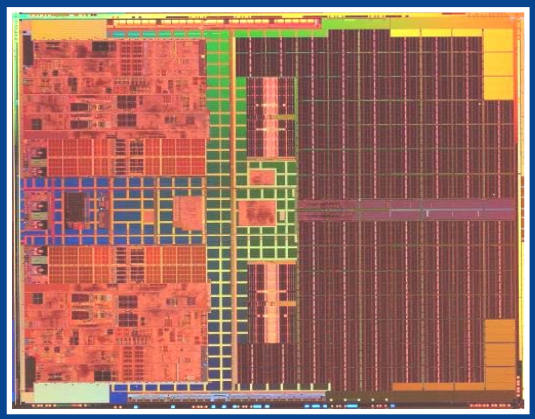
Intel® Pentium® Processor



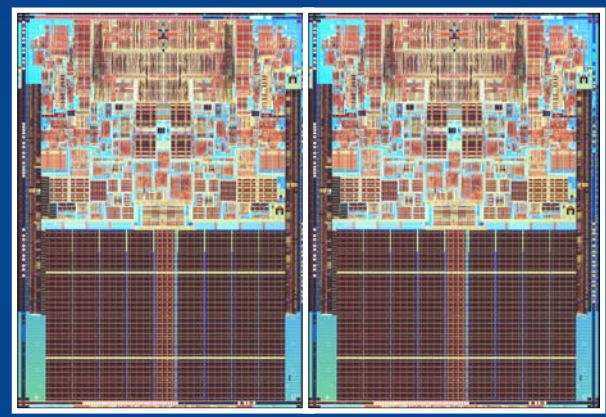
Intel® Core™ Duo Processor



Intel® Core™ 2 Duo Processor



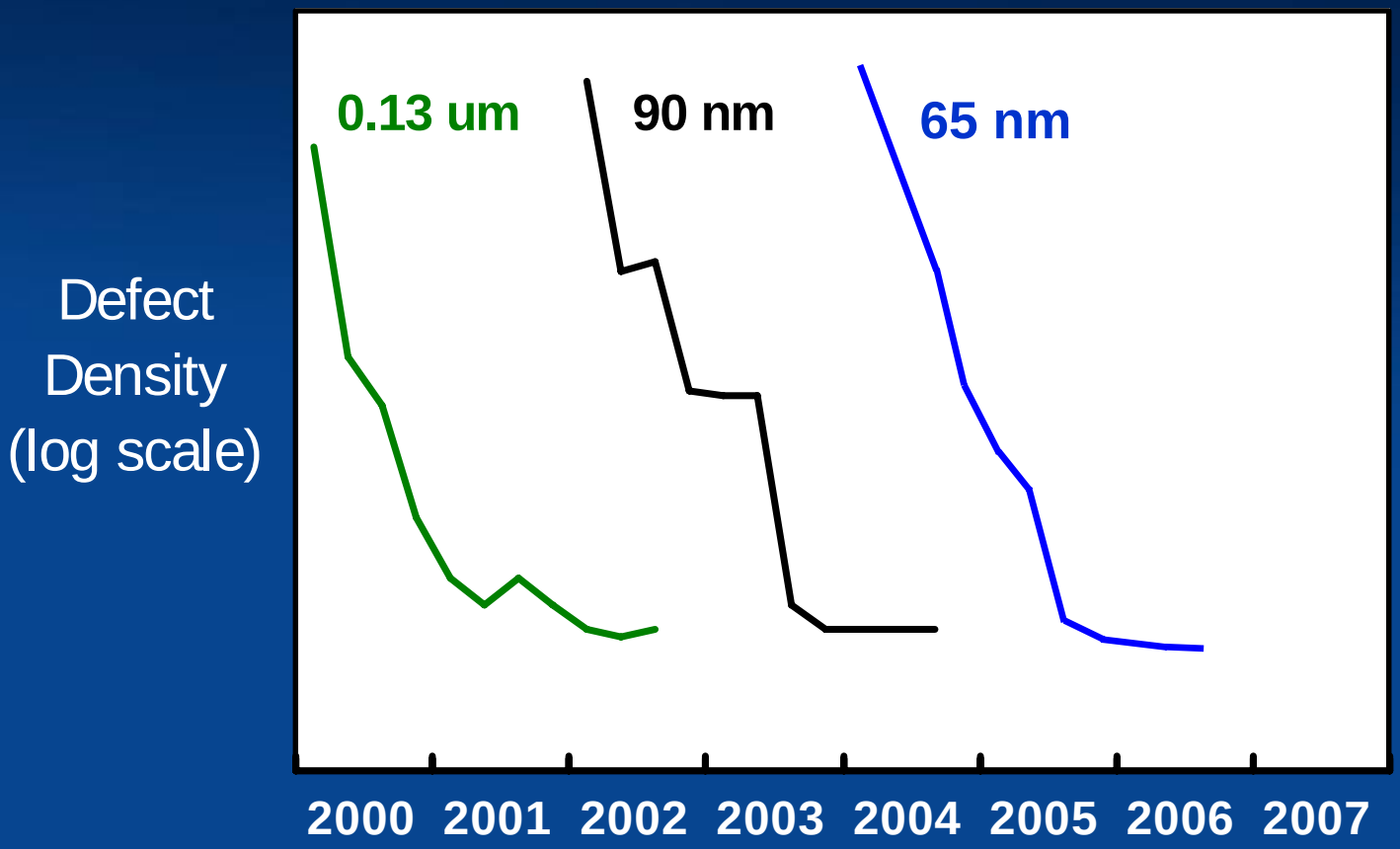
Dual-Core Intel® Xeon® 7100 Processor



Quad-Core Intel® Xeon® 5300 Processor

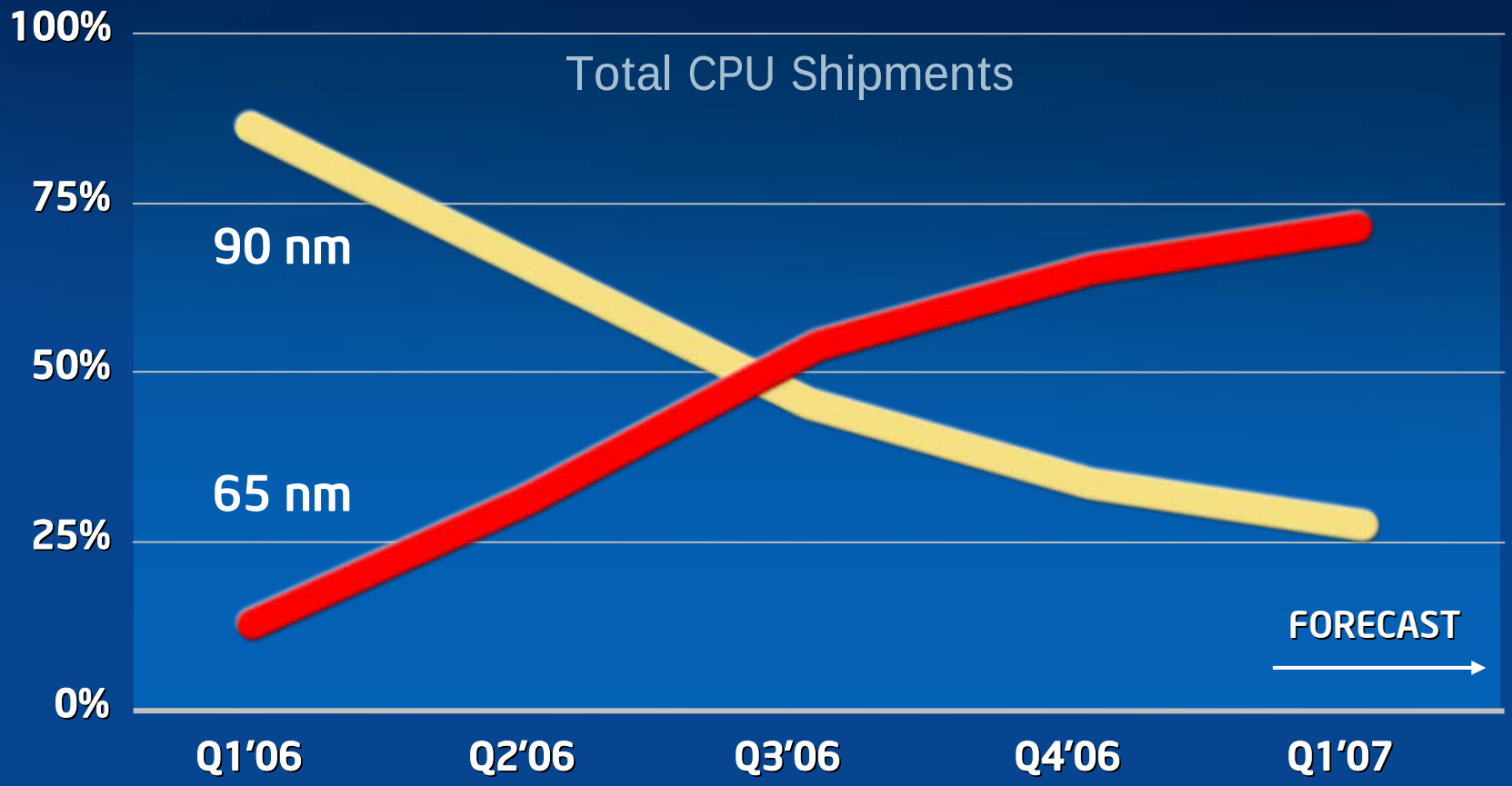
65 nm volume production started in October 2005

65 nm Yield Improvement Trend



65 nm is Intel's highest yielding process ever

Process + Products + Production



65 nm crossover occurred in Q3 '06

>120 million units shipped since 2005

Logic Technology Evolution

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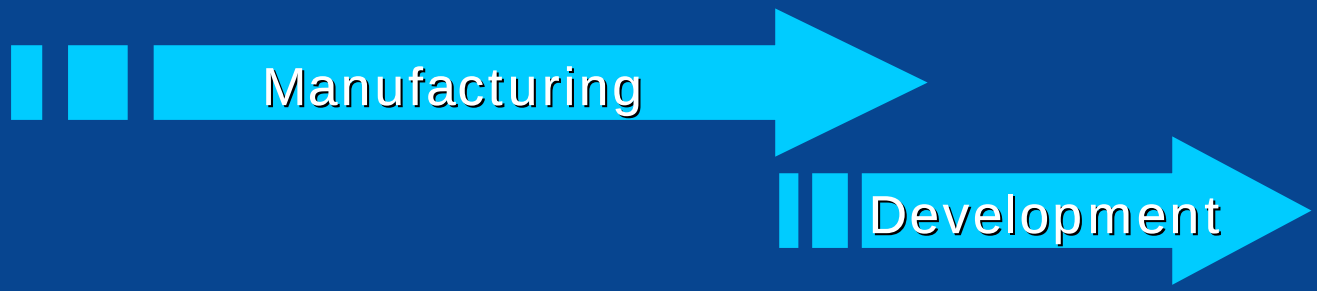
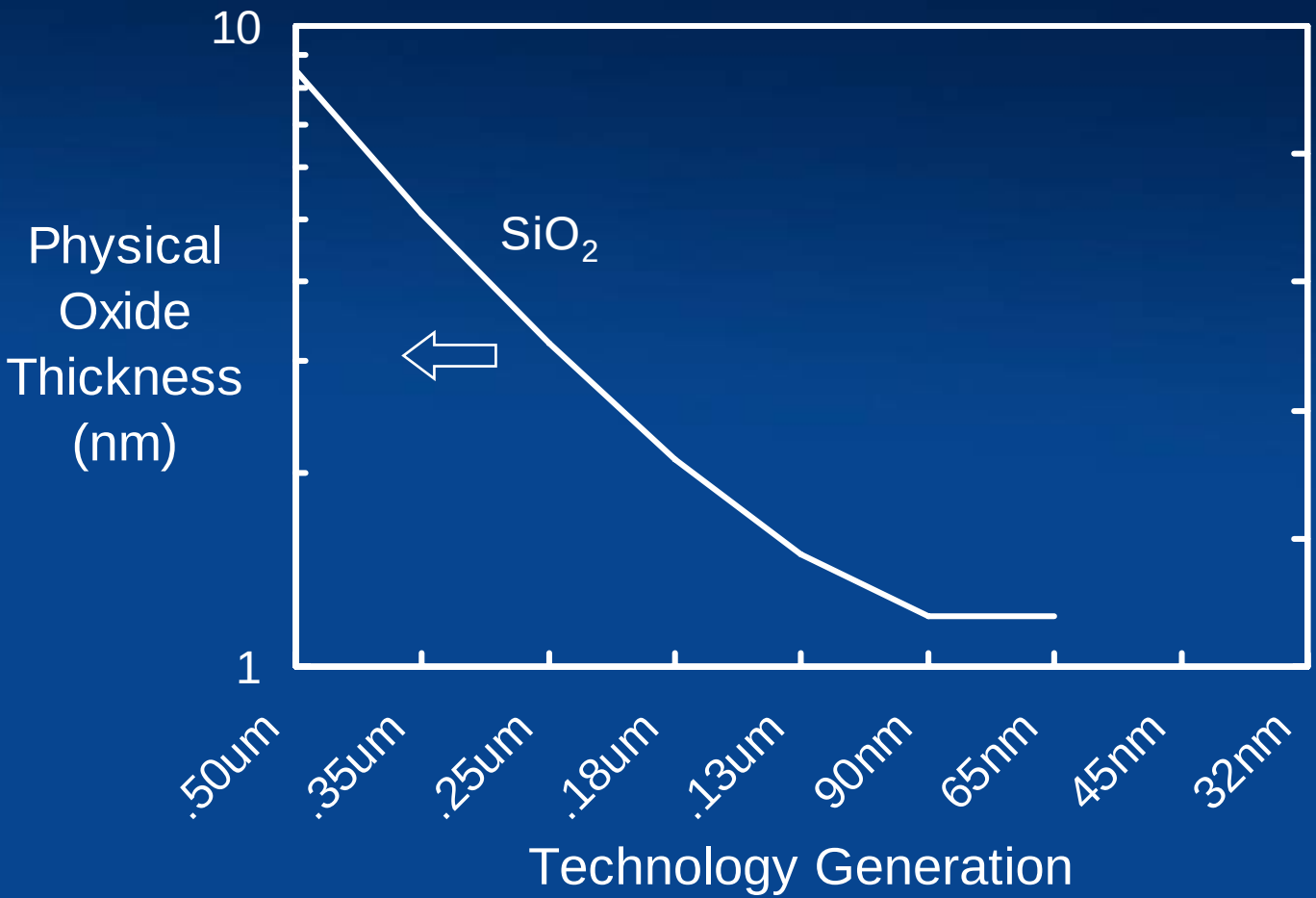


45 nm Technology Benefits compared to 65 nm

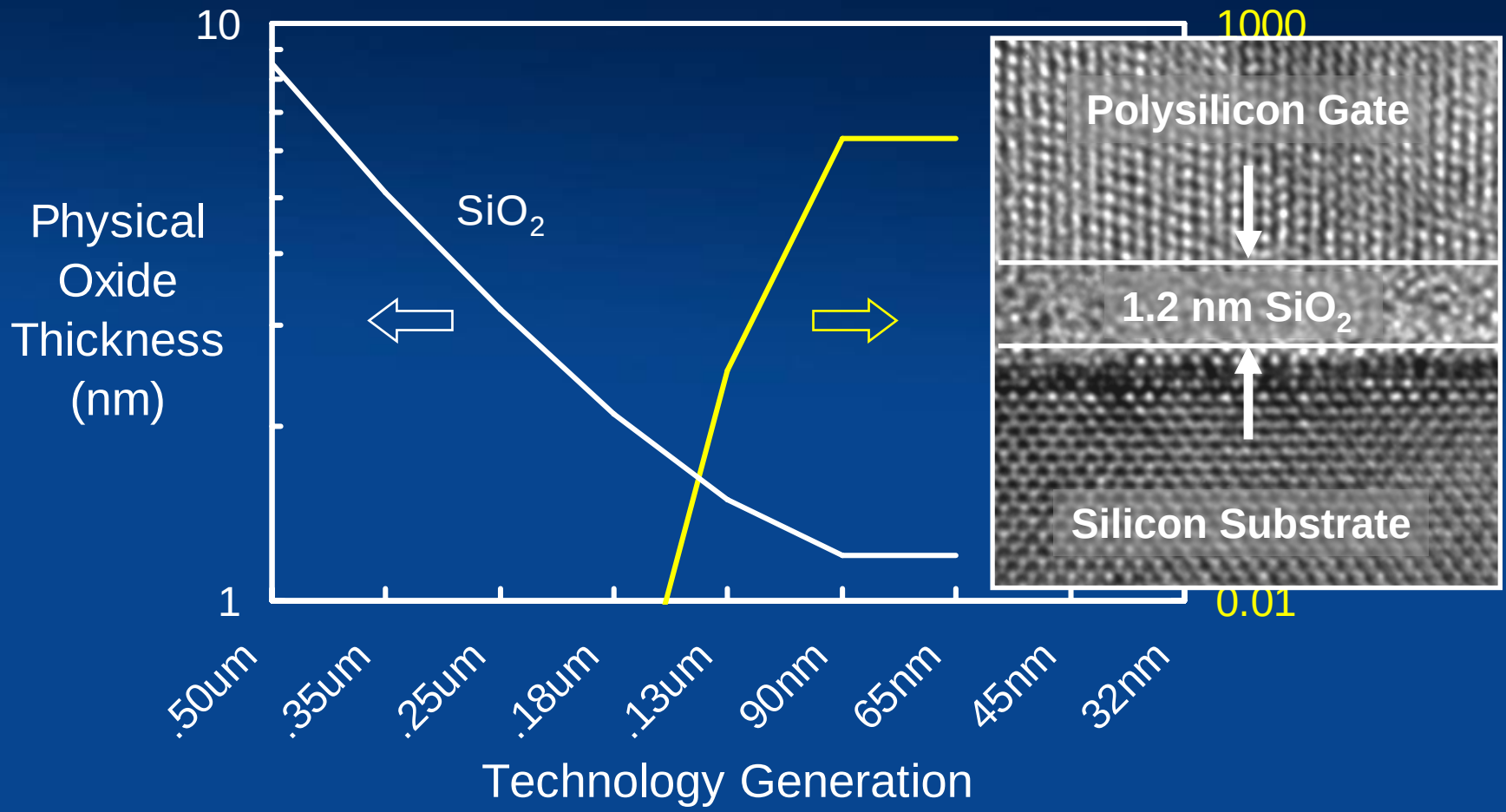
These performance and leakage improvements would not be possible without high-k + metal gate

~2x	improvement in transistor density, for either smaller chip size or increased transistor count
~30%	reduction in transistor switching power
>20%	improvement in transistor switching speed or
>5x	reduction in source-drain leakage power
>10x	reduction in gate oxide leakage power

Gate Oxide Scaling

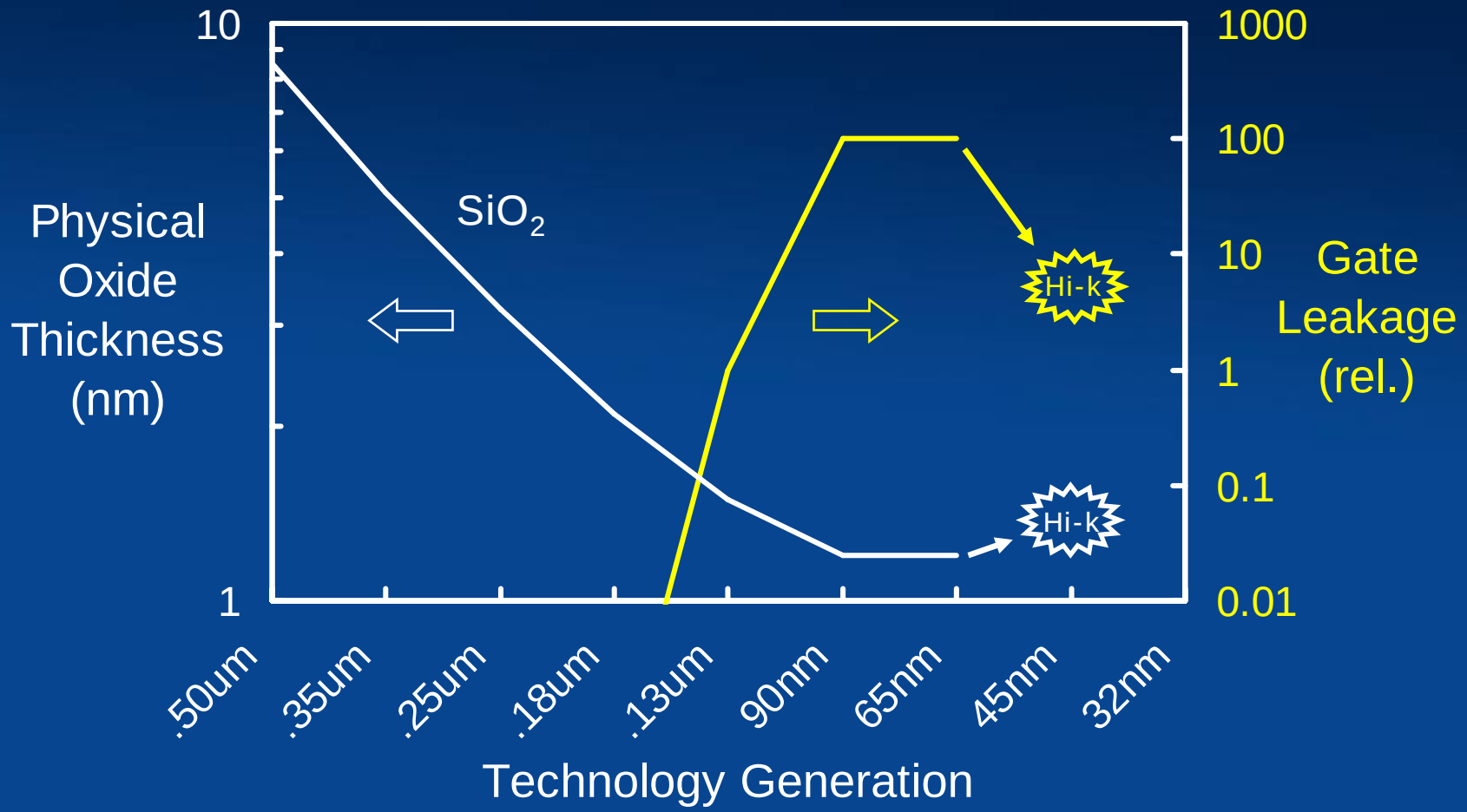


Gate Oxide Scaling



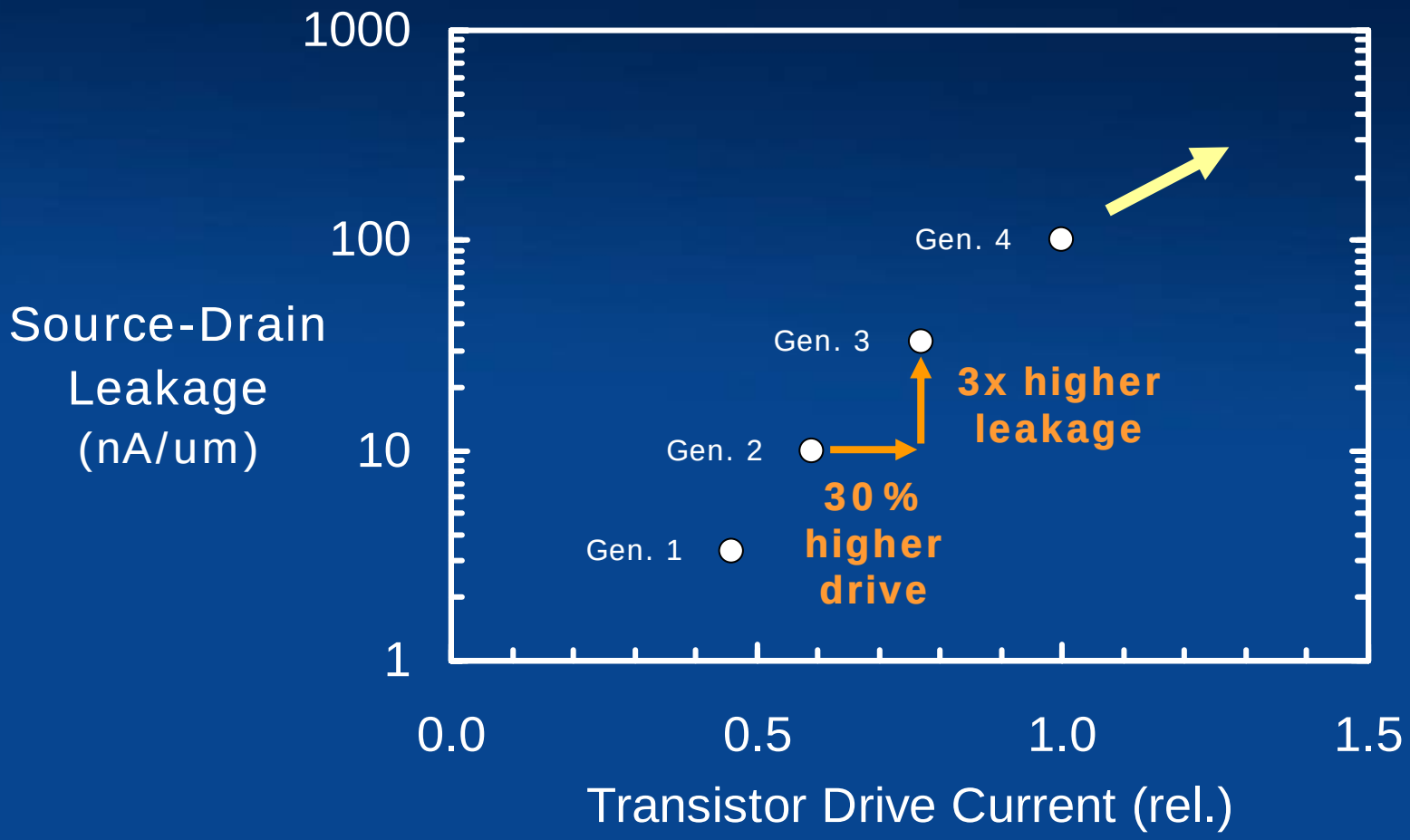
Gate oxide scaling stopped due to leakage

Gate Oxide Scaling



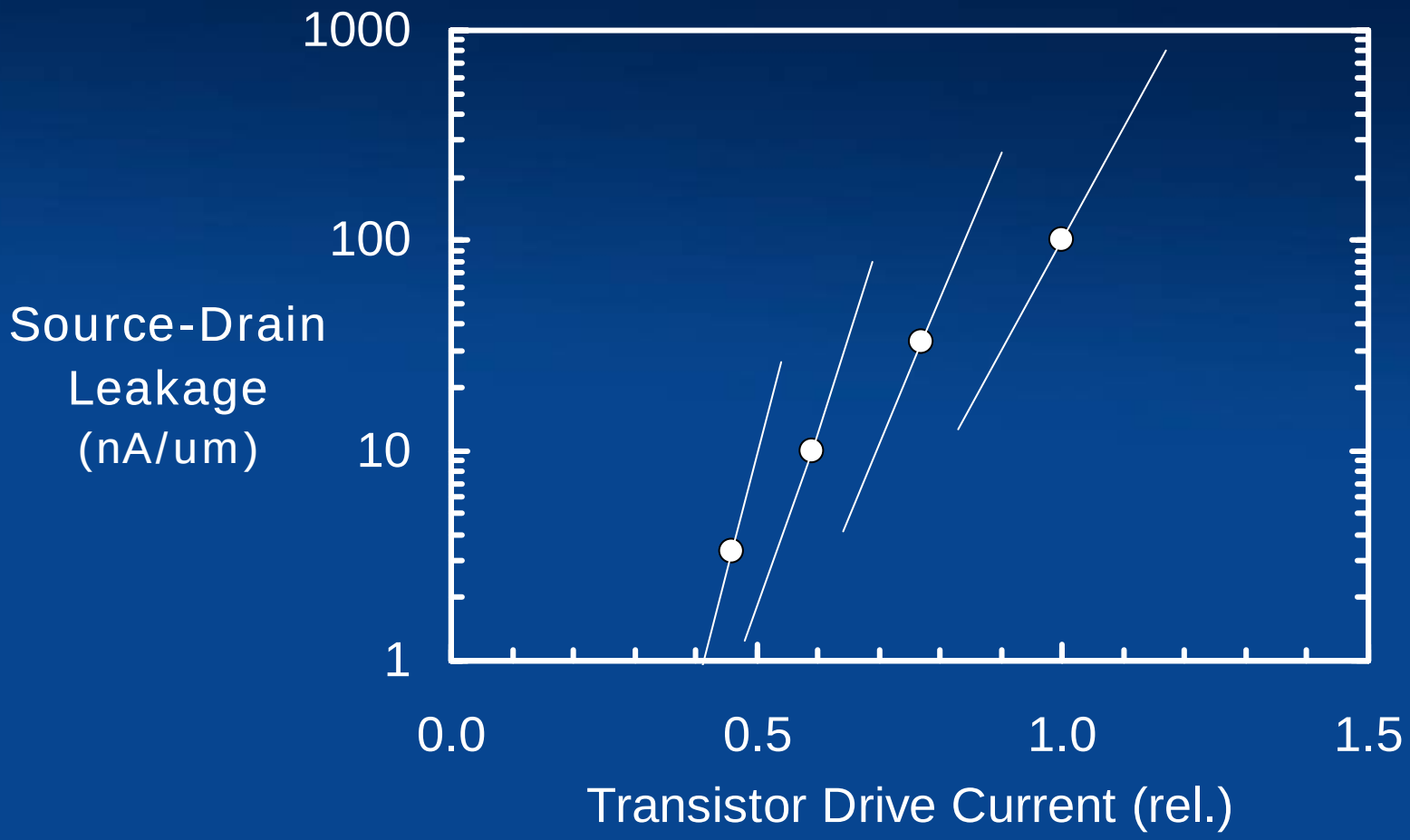
High-k dielectric breaks through this barrier

Transistor Performance vs. Leakage



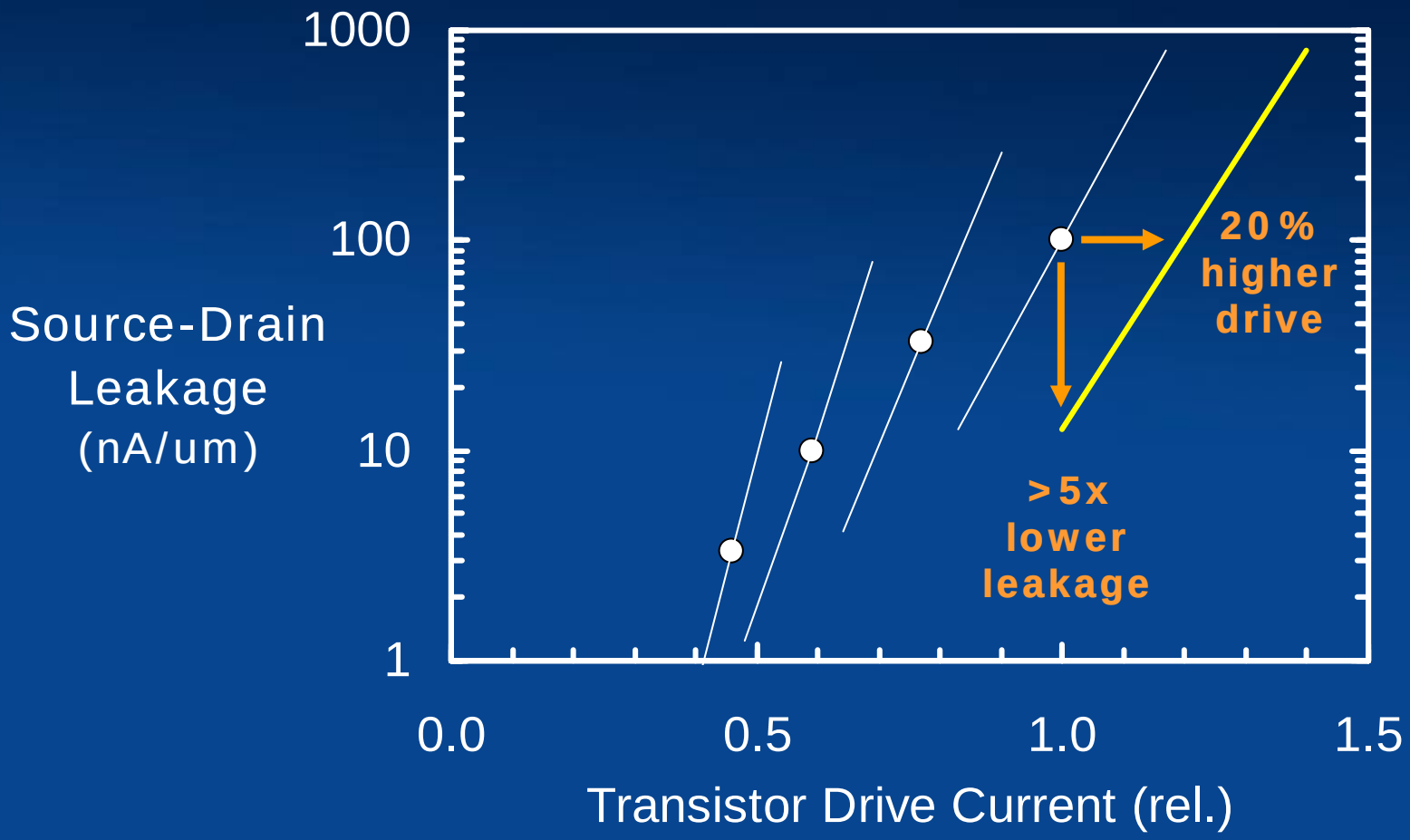
Historic source-drain leakage trend unsustainable

Transistor Performance vs. Leakage



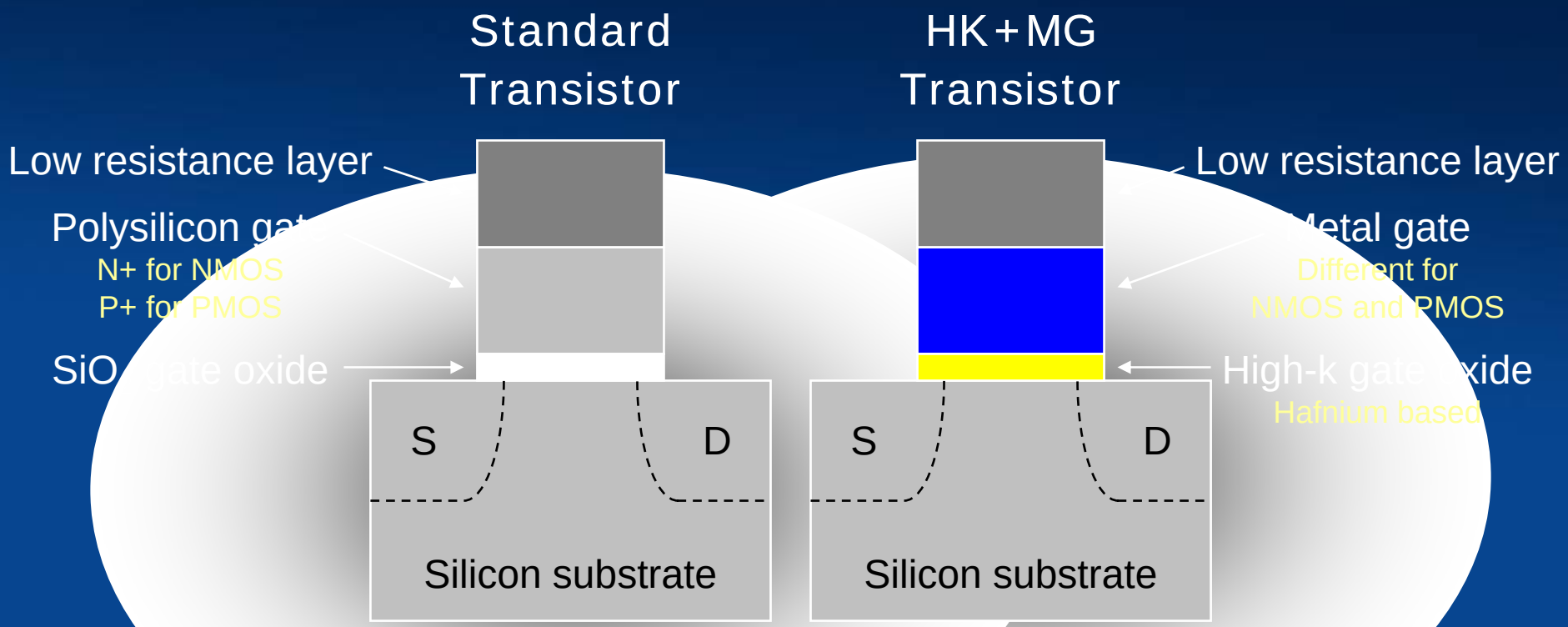
Range of drive current vs. leakage current

Transistor Performance vs. Leakage



45 nm high-k metal gate transistor benefits

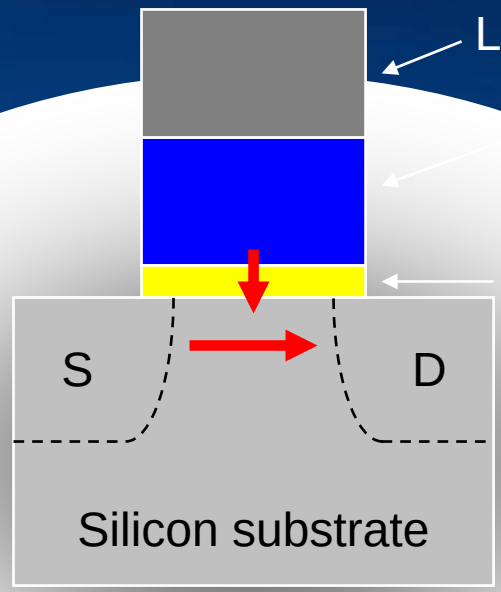
High-k + Metal Gate Transistors



High-k + metal gate transistors improve performance and reduce leakage, ensuring continuation of Moore's Law

High-k + Metal Gate Transistors

HK+MG
Transistor



Metal Gate

Increases the gate field effect

High-k Dielectric

Increases the gate field effect

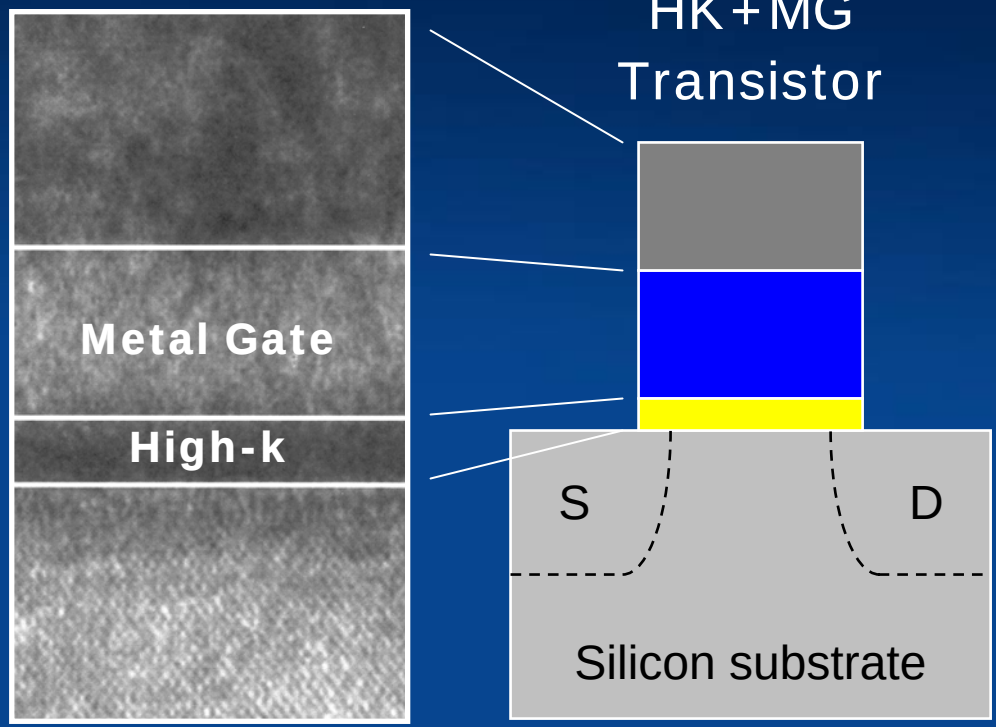
Allows use of thicker dielectric
to reduce gate leakage

High-k + Metal Gate Combined

Transistor drive current increased >20%
Or source-drain leakage reduced >5x
Gate oxide leakage reduced >10x

High-k + Metal Gate Transistors

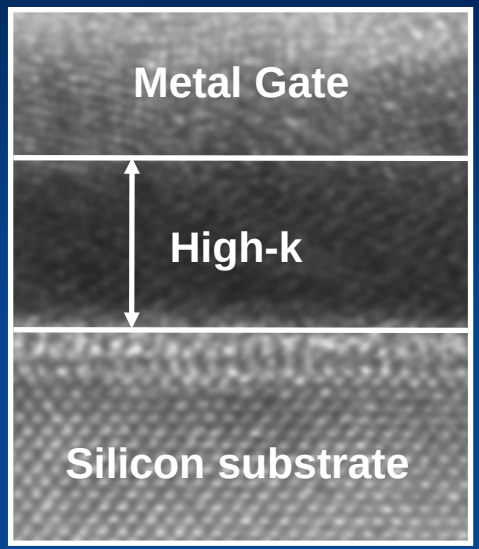
- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



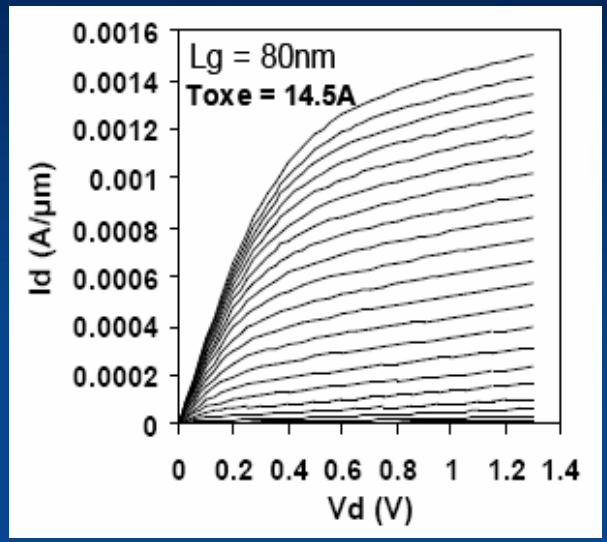
Biggest change in transistor technology in 40 years

intel

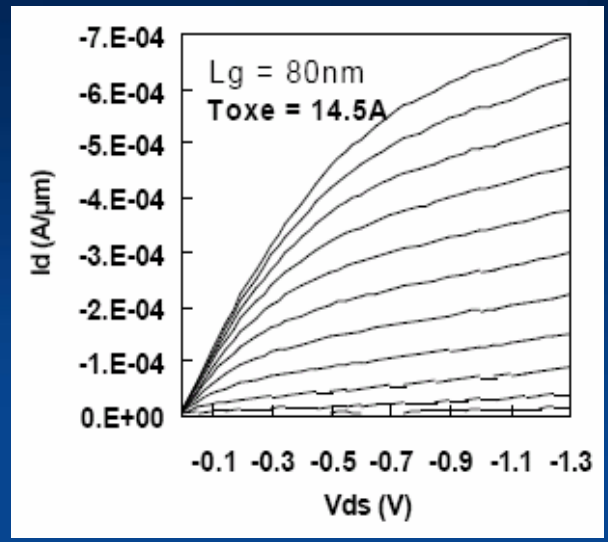
2003 High-k + Metal Gate Transistors



NMOS



PMOS



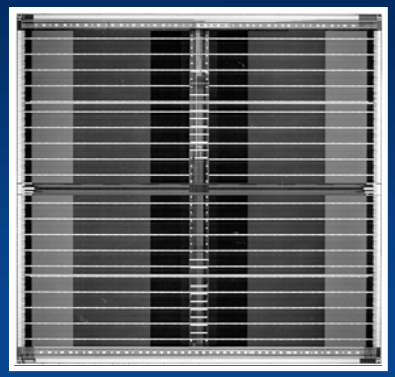
R. Chau, International Workshop on Gate Insulator, Tokyo, Japan, Nov. 2003

Intel 2007 for High-k Shift

By David Lammers, EE Times

November 10, 2003 – Intel Corp. last week said it has identified new gate stack materials – including a high-k oxide and two metals to replace polysilicon as the gate electrode – that could cut leakage current by as much as 100 times.

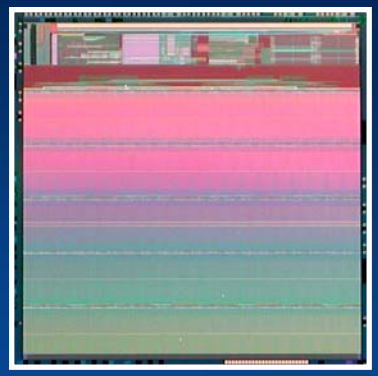
SRAM Test Chips



130 nm

18 Mbit

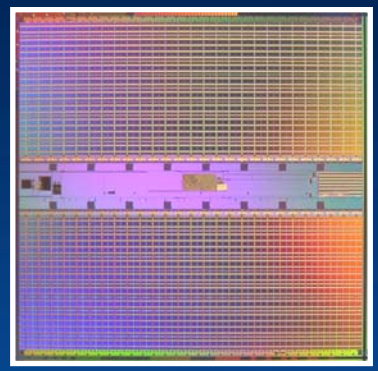
March ‘00



90 nm

50 Mbit

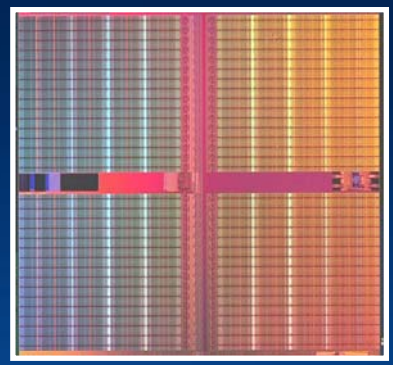
February ‘02



65 nm

70 Mbit

April ‘04



45 nm

153 Mbit

January ‘06

New SRAM test vehicle developed every 2 years
to lead development of logic technologies

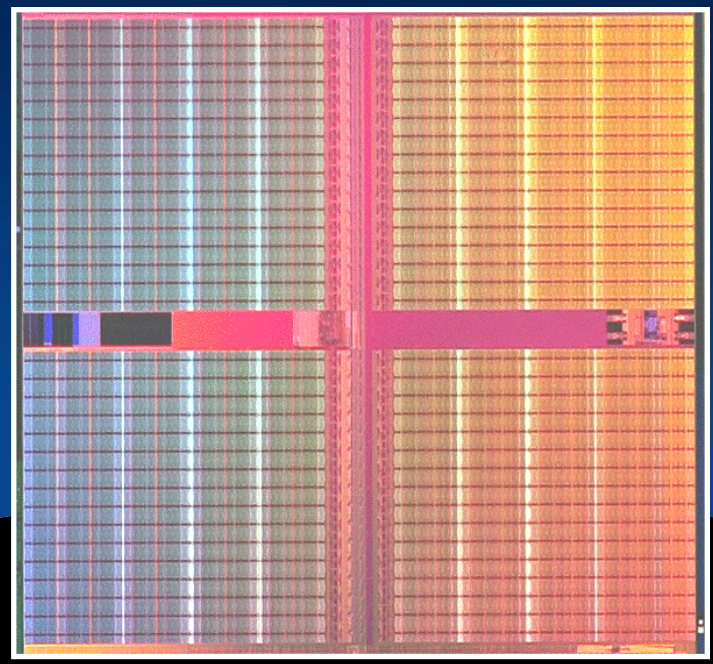
45 nm SRAM Test Chip

0.346 um^2 cell

153 Mbit density

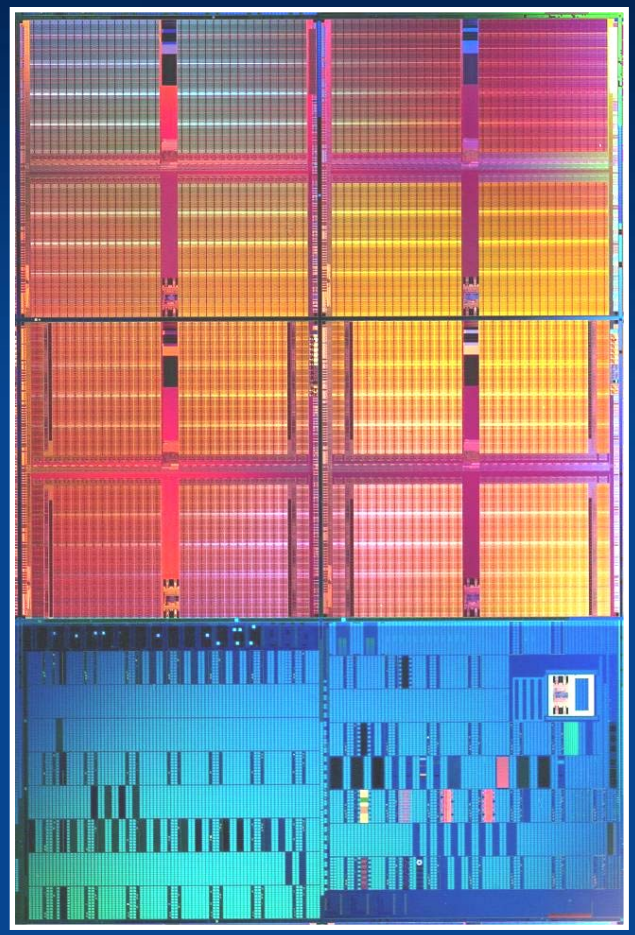
>1 billion transistors

Fully functional in Jan. ‘06



SRAM incorporated all process features used on
45 nm microprocessors, including high-k + metal gate

SRAM + Logic Test Chip



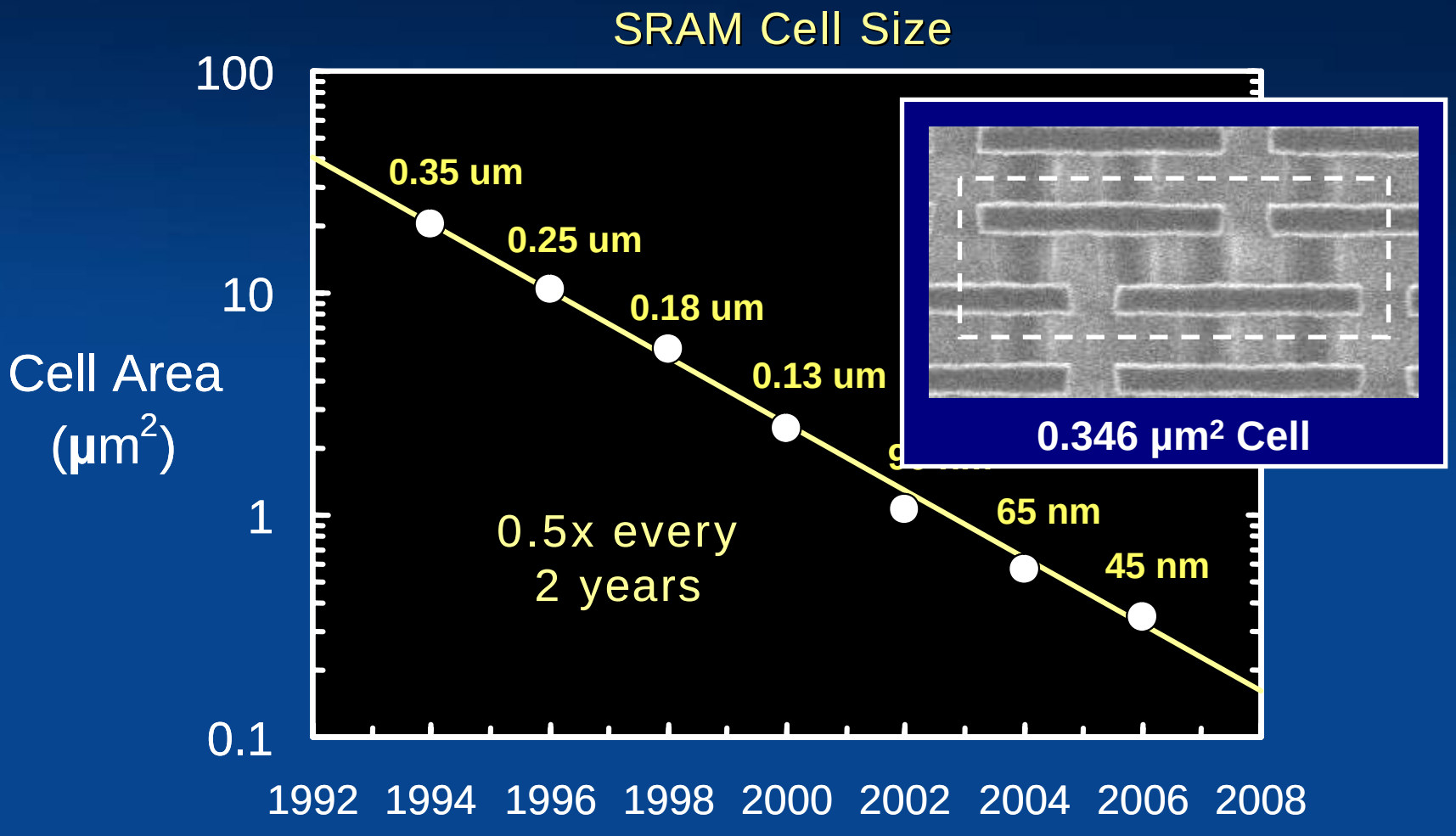
153M SRAM

SRAM array
PROM array
High speed register file
High speed I/O circuits
High frequency PLL/Clock

Discrete test structures

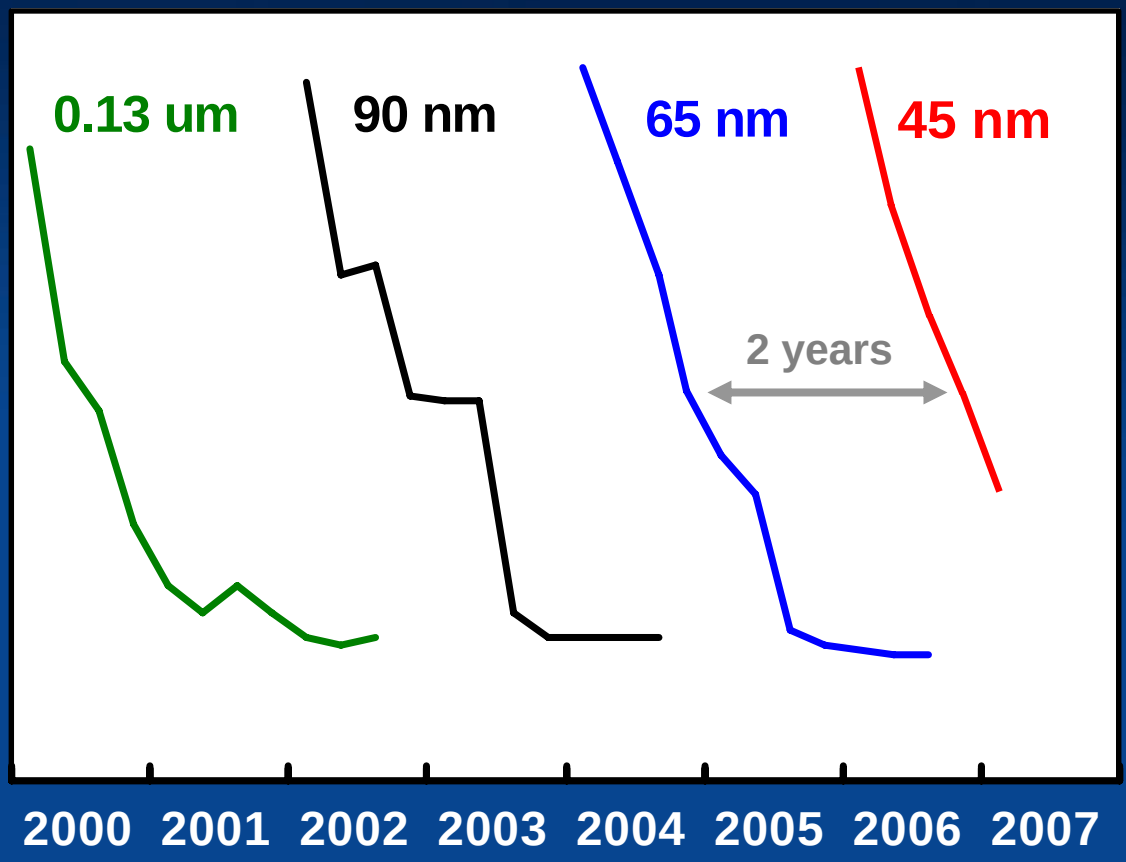
45 nm test chip included SRAM and logic circuits for CPUs

Density Scaling on Track



Cost-effective 193 nm dry lithography
extended to 45 nm generation

45 nm Yield Improvement Trend

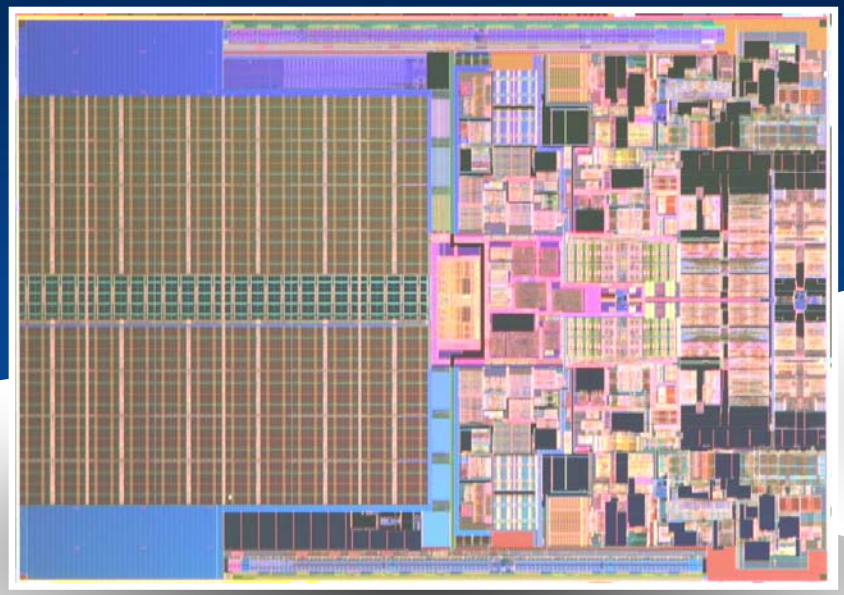


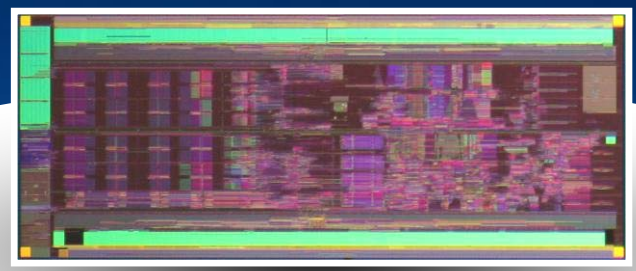
45 nm defect reduction trend at expected 2 year offset

45 nm on track for production in 2H ’07

Four factories coming on line in ’07 and ’08

World's First Working 45 nm CPUs





Penryn

45 nm Hi-k Intel® Core™2 and Intel Xeon™ processors

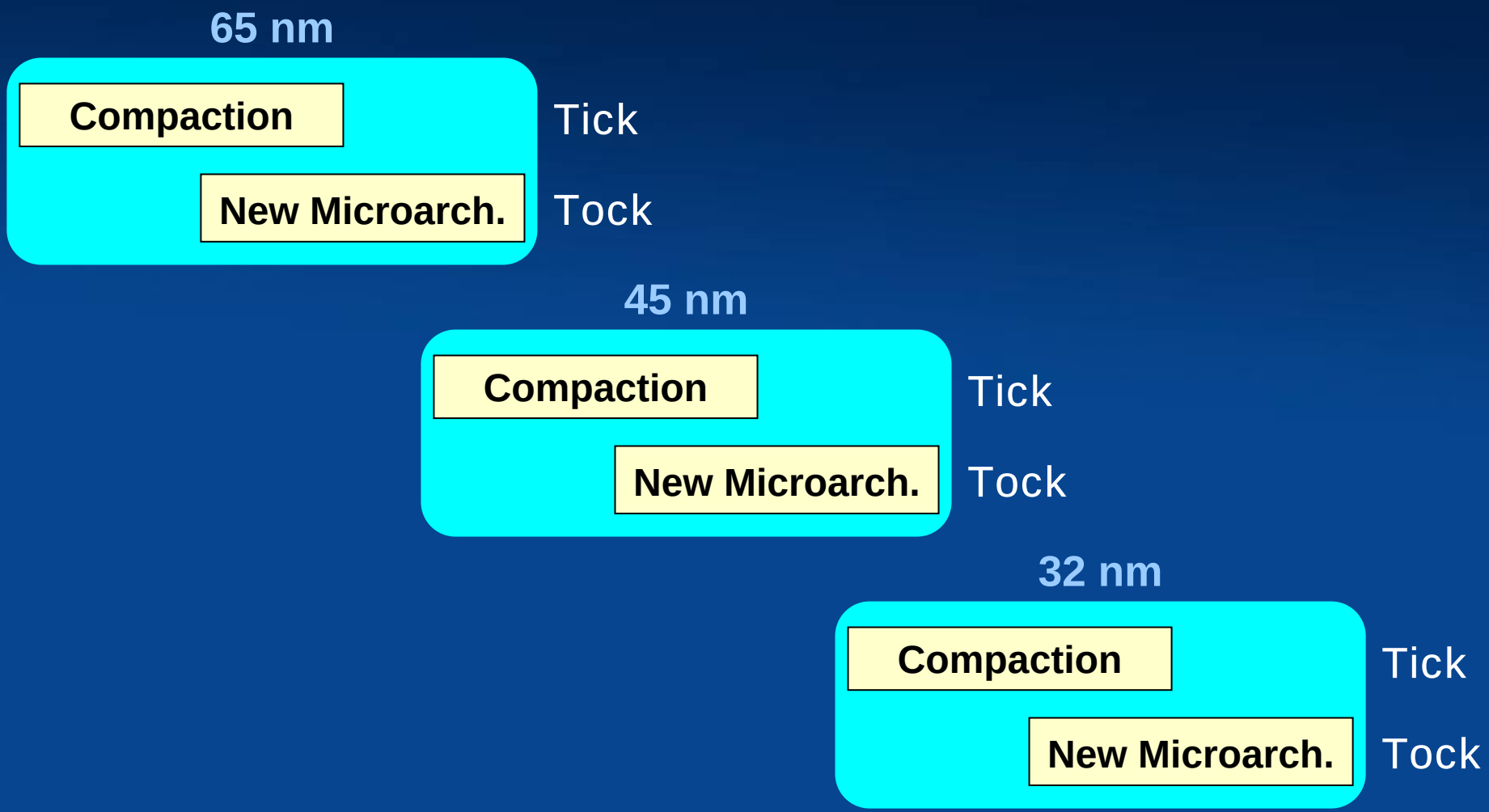
Mobile, Desktop, Workstation, and Server Optimized

Silverthorne

45 nm Hi-k new low power microarchitecture

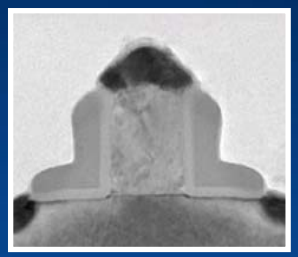
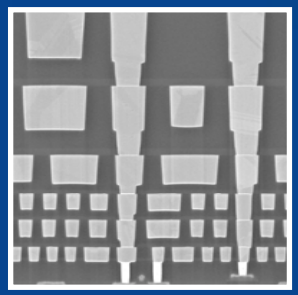
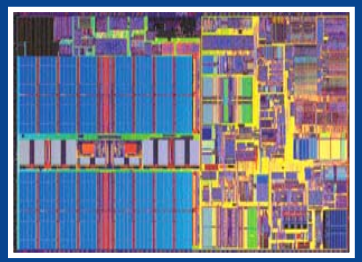
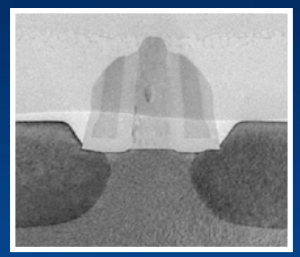
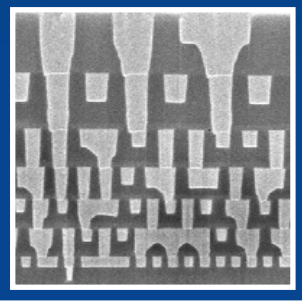
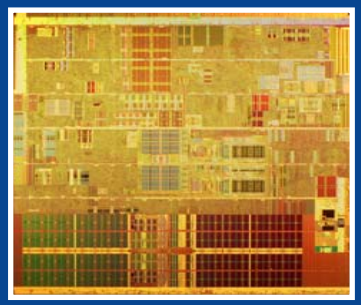
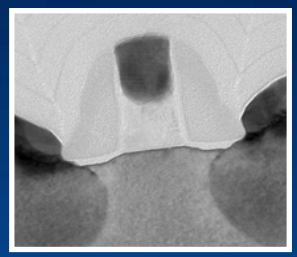
Mobile Internet Devices and Ultra-Mobile PCs

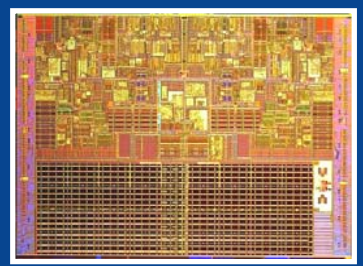
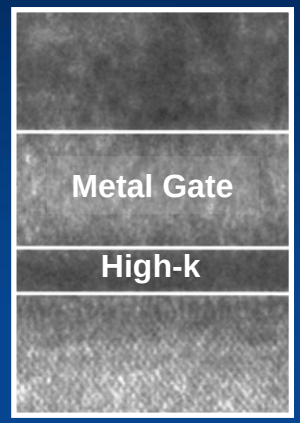
Tick-Tock Product Model

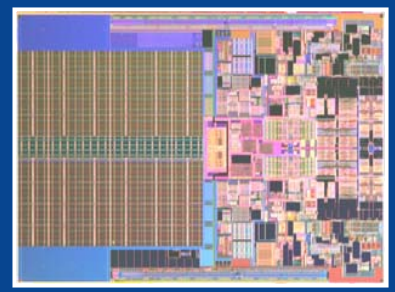


On-Time 2 Year Cycle

130 nm	90 nm	65 nm	45 nm
2001	2003	2005	2007



Reliable process and product introduction dates

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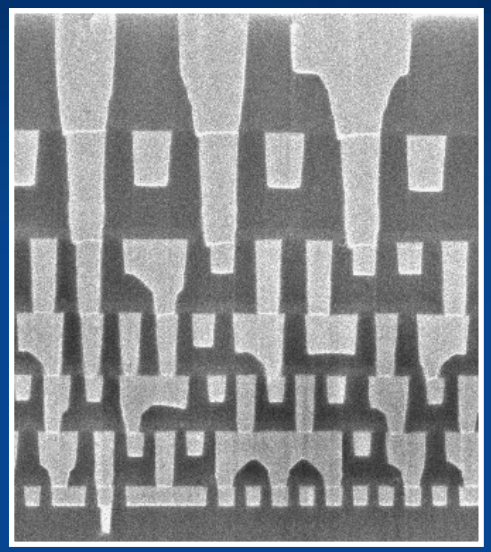
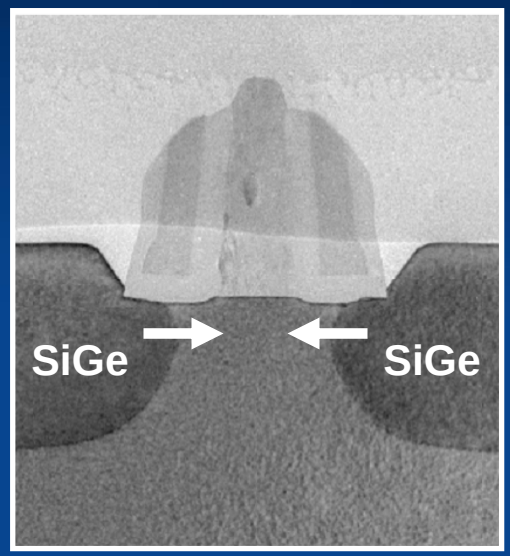
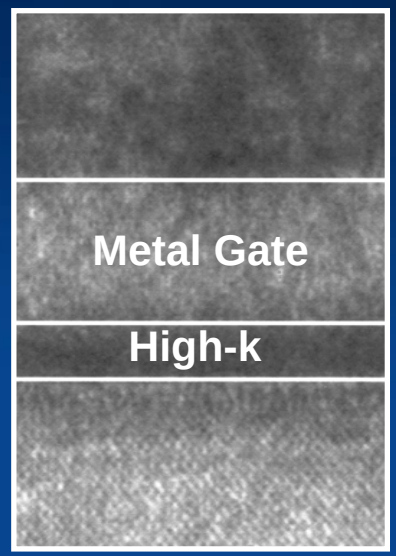
The New Era of Scaling



Copper + Low-k



Strained Silicon



High-k + Metal Gate

Modern CMOS scaling is as much about material innovation as dimensional scaling

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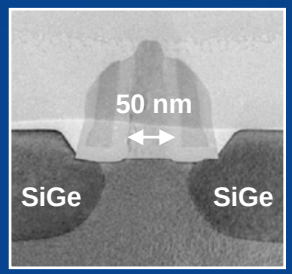
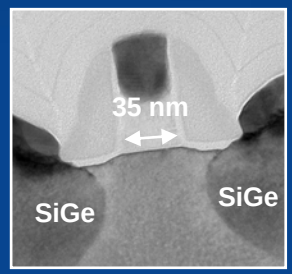
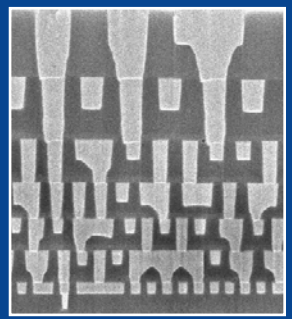
Innovation-Enabled Technology Pipeline

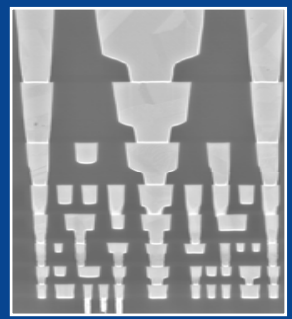
90 nm	65 nm	45 nm	32 nm	
2003	2005	2007	2009	2011+

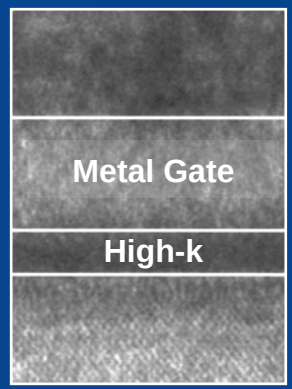
Manufacturing → **Development** → **Research**

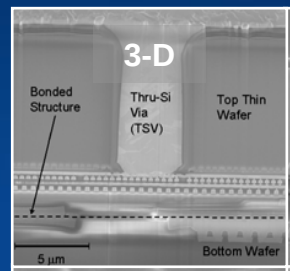


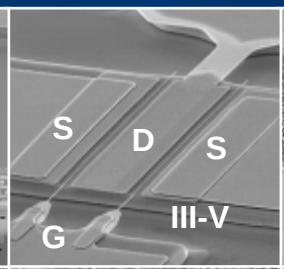


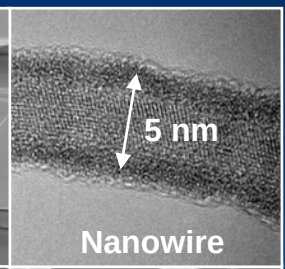


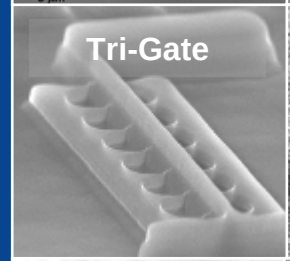


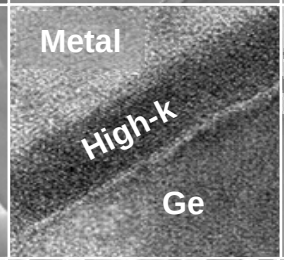


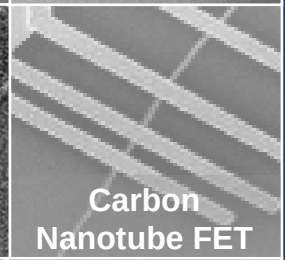


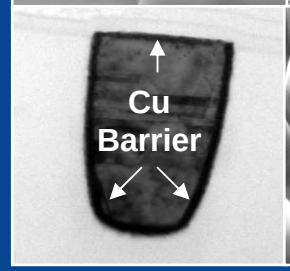


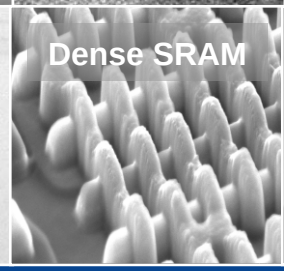


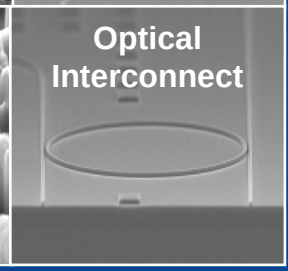












Future options subject to change

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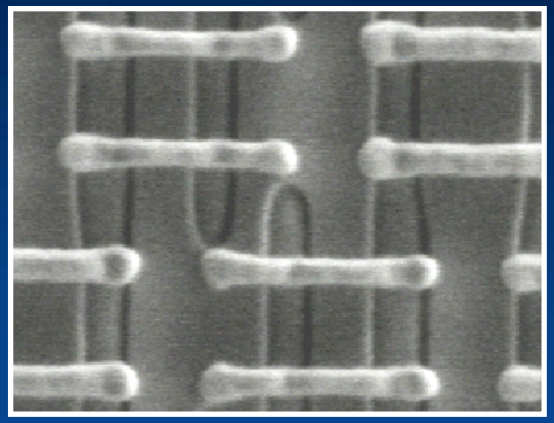
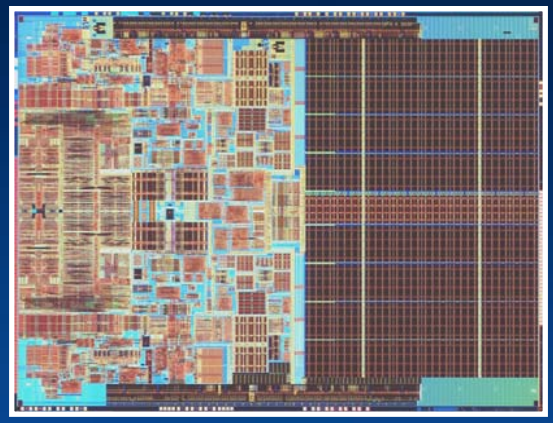
Intel's Comprehensive DFM

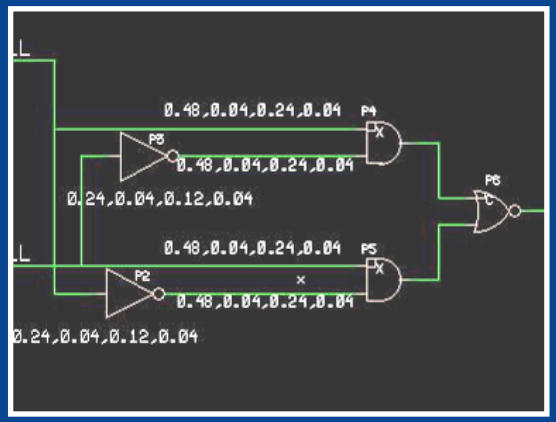


Process

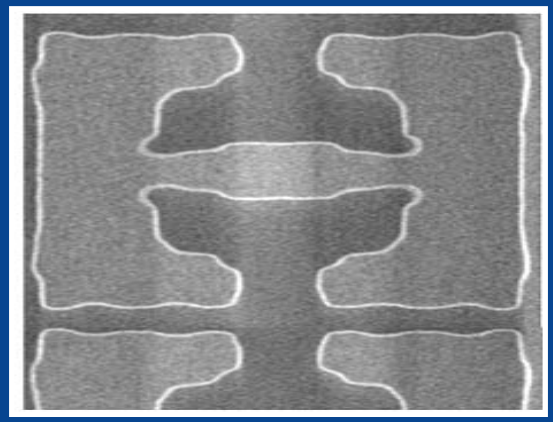


Products

Leading-edge Capacity



Design Tools



Masks

Packaging

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Summary

- Modern CMOS scaling is as much about material innovation as dimensional scaling
- 45 nm high-k metal gate is the most significant innovation in transistor technology in 40 years and delivers all three benefits of Moore's Law:
  - More transistors enable more functions
  - Cost-per-transistor goes down
  - Performance/watt goes up
- Intel continues its commitment to support R&D for future technologies and to deliver the benefits of Moore's Law to our customers